

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

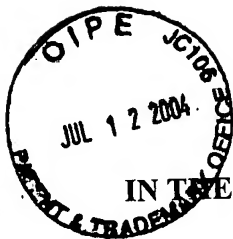
Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**



IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Tu

Application Serial No.: 10/618,793

Filed: July 15, 2003

For: Method of Improving the Top-Plate Electrode Stress Inducting Voids for IT-RAM Process

Patent No.:

Issue Date:

Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

**CERTIFICATE UNDER 37 C.F.R. §3.73(b)  
ESTABLISHING RIGHT OF ASSIGNEE TO TAKE ACTION**

1. The assignee of the entire right, title and interest hereby seeks to take action in the PTO in this matter.

**IDENTIFICATION OF ASSIGNEE**

2. The assignee of this matter is:

**TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.**  
8, Li-Hsin Rd. 6  
Hsinchu Science Park  
Hsinchu, Taiwan 300-77, R.O.C.

**PERSON AUTHORIZED TO SIGN**

3. Daniel R. McClure  
Attorney for Assignee

4. A chain of title from the inventor(s) to the current assignee is shown below:

- a. From: Kuo-Chi TU  
To: Taiwan Semiconductor Manufacturing Co., Ltd.  
Recorded in PTO: Reel: 014298 Frame: 0644
- b. From:  
To:  
Recorded in PTO: Reel: Frame:

### DECLARATIONS

5. I, the undersigned, have reviewed all the documents in the chain of title of the

- ☒ application  
☐ patent

matter identified above and, to the best of my knowledge and belief, title is in the assignee identified above.

6. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

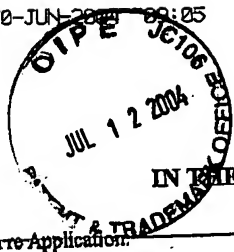
7. I, the person signing below, aver that I am empowered to sign this statement on behalf of the assignee.

  
Daniel R. McClure, Reg. No. 38,962

Tel. No. 770-933-9500  
Customer No.: 24504

**THOMAS, KAYDEN, HORSTEMEYER  
& RISLEY, L.L.P.**  
100 Galleria Parkway, Suite 1750  
Atlanta, Georgia 30339-5948

Docket No. 252016-1310



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:

Application No.:

Filed:

Title:

Commissioner for patents

Washington, D.C. 20231

**POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST  
(REVOCATION OF PRIOR POWERS)**

As assignee of record of each of the patent applications listed in the table of attachment A,

**REVOCATION OF PRIOR POWERS OF ATTORNEY**

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

**NEW POWER OF ATTORNEY**

the following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

**24504**

Patent Trademark Office

Please direct all future correspondence and telephone calls to:

Daniel R. McClure, Reg. No. 38,962

**THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.**

100 Galleria Parkway, Suite 1750

Atlanta, Georgia 30339

770-933-9500

**ASSIGNEE OF ENTIRE INTEREST****TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**

8, Li-Hsin Rd. 6


Hsinchu Science Park

Hsinchu, Taiwan 300-77, R.O.C.

**ASSIGNEE CERTIFICATION**

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Taiwan Semiconductor Manufacturing Company, Ltd., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

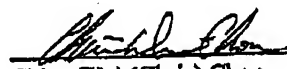
Date: June 29, 2004

  
Chien-Wei (Chris) Chou  
Director - Intellectual Property Division

## Attachment A

No.	Serial No	TSMC No.	Application Title	Filing Date	Assignment (Reel/Frame)
1	10/379,818	TS2001-1414	Novel Formation of an Aluminum Contact Pad Free of Plasma Induced Damage by Applying CMP	03/05/03	013849/0653
2	10/328,156	TS2001-897/1115	A Method to Fabricate a Square Word Line Poly Spacer	12/23/02	013627/0309
3	10/228,488	TS2002-0402	Methodology to Characterize Metal Sheet Resistance of Copper Damascene Process	08/27/02	013236/0138
4	10/618,793	TS2002-1284	Method of Improving the Top Plate Electrode Stress Inducing Voids for IT-RAM Process	07/15/03	014298/0644
5	10/284,984	TS2001-1045	ALSi <sub>x</sub> O <sub>y</sub> as a New Bi-Layer High Transmittance Attenuating Phase Shifting Mask Material for 193 Nanometer Lithography	10/31/02	013454/0219
6	10/444,875	TS2000-0763	Single Poly-Si Process for DRAM by Deep N Well (NW) Plate	05/23/03	014114/0996
7	10/154,740	TS2001-0672	A Method of Fabricating an ESD Device on SOI	05/24/02	012934/0775
8	10/639,884	TS2001-748/774/822B	Novel Silicon-Controlled Rectifier Structures on Silicon-On Insulator with Shallow Trench Isolation	08/13/03	recorded 012798/0129 at the parent application USP 6642088
9	09/889,837	TS2001-0071	RF Seal Ring Structure	11/20/01	012318/0614
10	10/696,430	TS2000-0680B	A Gate-Controlled, Negative Resistance Diode Device Using Band-to-Band Tunneling	10/29/03	recorded 012540/0729 at the parent application USP 6657240
11	10/308,447	TS2001-0921	Integrated Process Flow to Improve Copper Filling in a Damascene Structure	12/03/02	013557/0555
12	10/224,215	TS2001-0550	A Structure and Fabricating Method with Self-Aligned Bit Line Contact to Word Line in Split Gate Flash	08/20/02	013217/0778

Date: June 29, 2004

  
 Chien-Wei (Chris) Chou  
 Director - Intellectual Property Division